C.K. COLLEGE OF ENGINEERING AND TECHNOLOGY
Jayaram Nagar, Chellangkuppam, Cuddalore - 607 003.
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ANNA UNIVERSITY QUESTION PAPERS

Question Paper Code : 70085

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Third Semester

Electronics and Communication Engineering

EC 3352 — DIGITAL SYSTEMS DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Find the octal equivalent for the given decimal number $(149)_{10}$.

2. Simplify the Boolean function xy+x'z+yz to a minimum number of literals.

3. What is meant by combinational circuits? Give examples.

4. What is a parity bit?

5. Find the minimum number of flip flops required to build a modulo N counter.

6. Draw the master slave configuration using D-flip flop.

7. Differentiate between critical and non-critical race in asynchronous sequential circuits.

8. What is meant by fundamental mode sequential circuit?

9. Define fan in and fan out of a gate?

10. Write the difference between EPROM and EEPROM.

C.K. COLLEGE OF ENGINEERING & TECHNOLOGY * CUDDALORE 607 003

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PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the four variable boolean function F(A,B,C,D) = Σ(0,2,3,5,7,8,9,10,11,13,15) and find the prime implicants and essential prime implicants. (8)

(ii) Express the Boolean function F=xy+x'z as a product of maxterms. (5)

Or

(b) Minimize the expression Y(A,B,C,D)=Σm(0,1,3,7,8,9,11,15) using tabulation method.

12. (a) (i) Explain the working of 3-bit even parity generator and checker. (7)

(ii) Illustrate the operation of priority encoder. (6)

Or

(b) (i) Design a full adder and implement in sum-of-product form. (7)

(ii) Construct the 4 × 16 decoder with two 3 × 8 decoders. (6)

13. (a) Elucidate the analysis and design of clocked sequential circuits with a suitable example.

Or

(b) List out the capabilities of a universal shift register. Illustrate the four bit universal shift register with a function table and explain its working.

14. (a) Mention the types of hazard that occur in combinational circuits? Demonstrate the occurrence of static 0-hazard with a suitable example and find the solution to fix the static hazard in combinational circuits.

Or

(b) Taking relevant examples, explain the various types of races that occur in sequential circuits. Also briefly explain about the race free state assignment.

15. (a) Design the following sum-of-minterms using PAL.

$W(A,B,C,D)=\Sigma(2, 12, 13)$

$X(A,B,C,D)=\Sigma(7,8,9,10,11,12,13,14,15)$

$Y(A,B,C,D)=\Sigma(0,2,3,4,5,6,7,8,10,11,15)$

$Z(A,B,C,D)=\Sigma(1,2,8,12,13)$

Or

(b) (i) Draw and explain the totempole TTL output configuration. (6)

(ii) Compare the characteristics of RTL, TTL, ECL and CMOS logic families. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Design a counter using JK flip flops with the following binary sequence: 1, 2, 5, 7 and repeat.

Or

(b) Design the binary to gray code converter and draw the simplified logic diagram in sum-of-product form.

Reg. No. : | | | | | | | | | | | |

Question Paper Code : 30138

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Electronics and Communication Engineering

EC 3352 — DIGITAL SYSTEMS DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the decimal number 431 to binary.
2. State DeMorgan's theorem.
3. What is an encoder?
4. State the difference between parity generator and parity checker.
5. How are the outputs of Mealy model and Moore model decided?
6. What is a universal shift register?
7. When does a race condition exist in an asynchronous sequential circuit?
8. What is the cause of an essential hazard?
9. Define noise margin.
10. List the types of ROMs with their expansion.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Simplify the Boolean function $(BC'+A'D)(AB'+CD')$ to a minimum number of literals. (6)

(b) Describe various types of hazards and the methods to eliminate hazards in combinational and sequential circuits. (13)

15. (a) (i) Draw and explain CMOS logic circuits. (7)

(ii) Explain a TTL gate with totem pole output. (6)

Or

(b) (i) Using 64 × 8 ROM chips with an enable input, construct a 512 × 8 ROM with 8 chips and a decoder. (7)

(ii) Draw a PLA circuit to implement the functions (6)

$F_1 = A'B + AC + A'BC'$

$F_2 = (AC + AB + BC)'$

PART C — (1 × 15 = 15 marks)

16. (a) Simplify the following Boolean function by using the tabulation method.

$F = \sum(0,1,2,8,10,11,14,15)$ (15)

Or

(b) A sequential circuit has two JK flip flops A and B and one input X. The circuit is described by the following flip flop input equations.

$J_A = x \qquad K_A = B$

$J_B = x \qquad K_B = A'$

(i) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables. (8)

(ii) Draw the state diagram of the circuit. (7)

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Question Paper Code : 20925

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Third Semester

Electronics and Communication Engineering

EC 3352 – DIGITAL SYSTEMS DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Show the logic function of the Venn diagram shown in Fig. 1.

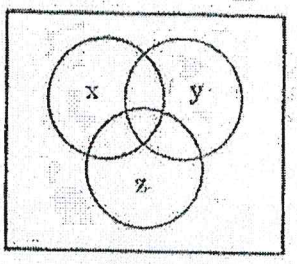

Fig. 1

2. A burglar alarm for a bank is designed so that it senses four input signal lines. Line A is from the secret control switch, line B is from a pressure sensor under a steel safe in a locked closet, line C is from a battery-powered clock, and line D is connected to a switch on the locked closet door. The following conditions produce a logic 1 voltage on each line:

   (a) The control switch is closed.

   (b) The safe is in its normal position in the closet.

   (c) The clock is between 1000 and 1400 hours.

   (d) The closet door is closed.

   Write the equations of the control logic for the burglar alarm that produces a logic 1 (rings a bell) when the safe is moved and the control switch is closed, or when the closet is opened after banking hours or when the closet is opened with the control switch open.

3. Obtain the logic circuit diagram for a 4-line to 2-line priority encoder. Include an output V to indicate that at least one input is a 1.

4. Obtain the logic circuit diagram for a 4-bit odd parity checker.

5. A certain J-K flip-flop has tpd = 12 ns. What is the largest MOD counter that can be constructed from these flip-flops and still operate up to 10 MHz?

6. Design an n-bit Johnson counter.

7. List the general requirements for Essential hazard formation.

8. Differentiate critical and noncritical race.

9. Calculate noise margin low and noise margin high for the following voltage levels.

   VOH = 3.5V, VOL = 0.45 V, VIH = 2.35V, VIL = 0.66 V.

10. Write the working principle of EPROM.

PART B — (5 × 13 = 65 marks)

11. (a) Design a 4-bit Binary-Coded Decimal (BCD) input/single output logic circuit that will be used to distinguish digits that are greater than or equal to 5 from those that are less than 5. The input will be the BCD representation of the decimal digits 0,1...9, and the output should be 1 if the input is 5, 6, 7, 8, or 9 and 0 if the input is less than 5. Obtain the following.

    (i) Minimum SOP form

    (ii) Minimum POS form.

Or

(b) Use the tabular procedure to simplify the give expression

F(V, W, X, Y, Z) = m(0, 4, 12, 16, 19, 24, 27, 28, 29, 31) in SOP form and draw the circuit using only NAND gates.

12. (a) Design a 4-bit adder that should have a computational complexity of O(1).

Or

(b) Design a logic circuit that compares two 4-bit inputs A and B and produces their relative magnitudes.

13. (a) Deduce a logic circuit diagram to produce the following sequences of input and output signals.

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	1	0	0	1	1	0	0

Or

(b) A universal shift register can shift in both the left-to-right and right-to-left directions, and it has parallel-load capability. Draw a circuit for such a shift register.

14. (a) What is a flow table? Derive a logic circuit diagram for the flow table given below.

	$x_1 x_2$ = 00	01	11	10
a	(a), 0	(a), 0	(a), 0	b, 0
b	a , 0	a , 0	(b), 1	(b), 0

Or

(b) Using tabular method, reduce the number of states in the state table given below.

	x y		q*		
q	0 0	0 1	1 0	1 1	Z
A	B	A	F	D	1
B	E	A	D	C	1
C	A	F	D	C	0
D	A	A	B	C	1
E	B	A	C	B	1
F	A	F	B	C	0

15. (a) Discuss about the various programmable logic devices and implement the following functions using PLA.

F1 = (AB + AC + BC)'

F2 = AB + AC + A'B'C'

Or

(b) Compare and contrast the features of TTL and CMOS logic styles and implement XOR and XNOR gates using CMOS logic style.

PART C — (1 × 15 = 15 marks)

16. (a) Design a digital combinational lock using pulse mode sequential circuit that takes two inputs X and Y and produces two outputs Lock and Open. The input pulse sequence required to open the lock is X-X-Y-X-Y. Implement the next state and output forming logic using a ROM.

Or

(b) Design a 4-bit ALU to perform the following arithmetic and logic operations.

- Transfer A
- Increment A
- Addition
- Addition with carry
- Subtract with borrow
- Subtraction
- Decrement A
- Transfer A
- OR
- XOR
- AND
- Complement A.